Internal Microwave Propagation and Distortion Characteristics of Traveling-Wave Amplifiers Studied by Electrooptic Sampling

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Abstract —**The internal signal propagation and saturation characteristics of two monolithic microwave traveling-wave amplifiers (TWA) are measured by electrooptic sampling. Gate and drain line responses are compared with theory and simulation, leading to revisions in the FET models. Drain voltage frequency dependence and harmonic current propagation together lead to more complex saturation behavior than is discussed in the literature.**

I. Introduction

THE FREQUENCY RESPONSE and distortion characteristics of monolithic traveling-wave amplifiers (TWA) depend upon the propagation characteristics of microwave signals along the gate and drain transmission lines. The bandwidth and gain flatness of the amplifier are set by the finite cutoff frequencies of the periodically loaded lines, the line losses due to FET input and output conductances, and the mismatch between gate and drain propagation velocities. The gain compression characteristics are set by several saturation mechanisms in the transistors, by the power at which each mechanism occurs in each FET, and by the propagation of both the amplified signal and the generated distortion products. While some of these factors are considered in the modeling and design of a TWA, the model can be verified only by measurement of the amplifier's external scattering parameters; if an amplifier does not perform to expectations, the cause is not easily identified. If the voltages at the internal nodes of the amplifier could be measured, the amplifier's characteristics would be much better understood. Such measurements are now possible using electrooptical techniques.

II. Electrooptic Sampling

We have developed a system for direct electrooptic sampling in GaAs integrated circuits [1]–[4]. In contrast to the external approach of Valdmanis *et al.* [5], our system, which measures the electric-field-induced changes in polarization of picosecond pulses of subbandgap laser radiation as they pass through the GaAs substrate of the IC, can noninvasively measure the voltages at arbitrary points within the circuit. The sampler currently has a bandwidth of 80 GHz, a timing drift of 0.5 ps/min, a measured noise floor of -60 dBm (1 Hz), and a spatial resolution of 3–10 μm, depending upon the focusing lens. The sampler can be configured to emulate either a sampling oscilloscope or a network analyzer.

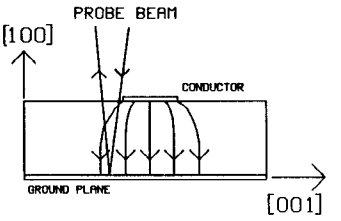

Fig. 1. Sampling geometry used for probing microstrip transmission lines.

GaAs is electrooptic; thus, the electric fields associated with conductor voltages induce optical birefringence, causing a small change in polarization to a subbandgap optical probe beam passing through these fields. The polarization change can be detected by passing the probe beam through a polarizer and onto a photodetector. Probing geometries for measuring the voltage on microstrip and coplanar transmission lines are shown in Figs. 1 and 2, respectively.

Fig. 3 shows the sampling system. A mode-locked Nd:YAG laser is driven at 82 MHz, producing optical pulses of 1.06-μm wavelength and 100-ps duration. A fiber-grating pulse compressor reduces the pulse duration to 2 ps and a phase-lock-loop timing stabilizer reduces the laser timing jitter to 1 ps. The probe beam passes through a polarizing beamsplitter and a $\lambda/4$ waveplate whose major axis is oriented at 22.5° to the axis of the beamsplitter, producing an elliptical polarization. The ellipse major axis is aligned at 45° to the electrooptic axes of the GaAs IC substrate by a $\lambda/2$ waveplate placed between the quarter-waveplate and the circuit. The beam is focused by a 5× microscope objective adjacent to or on the conductor of interest for the microstrip or coplanar geometries, respectively.

Manuscript received March 28, 1986; revised June 18, 1986. This work was supported by the Air Force Office of Scientific Research under Contract F496 20-85K-0016. M. Rodwell's research was supported by an IBM Fellowship.

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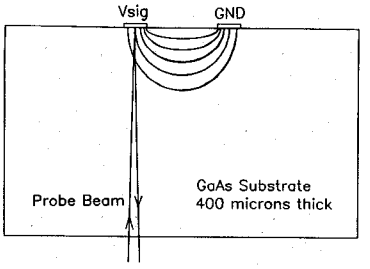

Fig. 2. Backside reflection geometry used for probing coplanar waveguide, coplanar strips, or lumped-element interconnects.

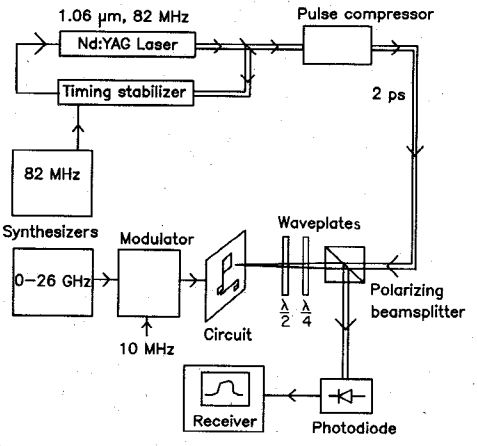

Fig. 3. Electrooptic sampling system.

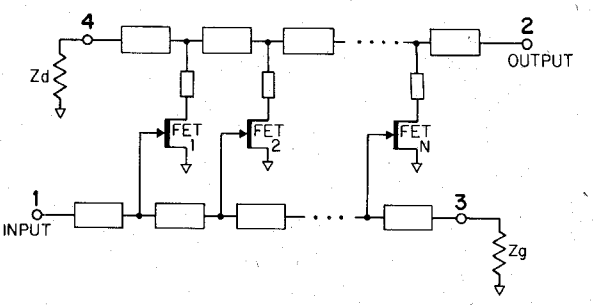

Fig. 4. Traveling-wave amplifier topology.

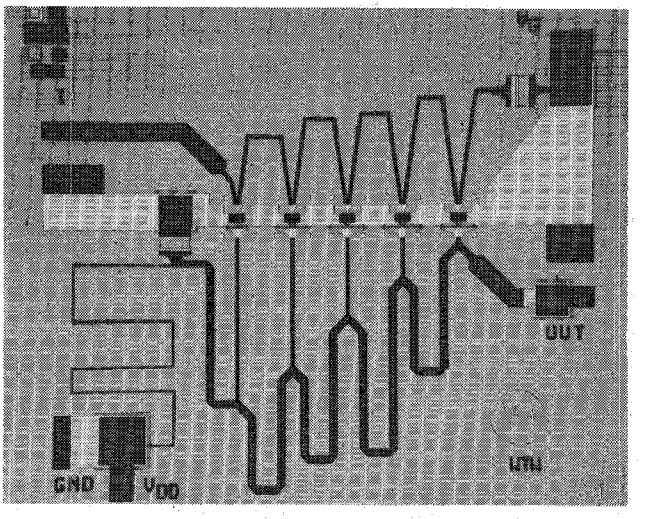

Fig. 5. 2–18-GHz TWA using microstrip transmission lines.

The reflected beam passes back through the waveplates, producing a linear polarization rotated at 45° to the axes of the beamsplitter; the polarization component of the beam at 90° orientation is directed by the beamsplitter onto a photodiode connected to a receiver. Through the electrooptic effect, the probed conductor voltage on the IC perturbs the polarization of the returning beam, changing the intensity of the beam incident upon the photodiode.

The circuit under test is driven by a microwave synthesizer whose output is pulse modulated at 10 MHz, allowing synchronous detection with a narrow-band 10-MHz double-sideband receiver at a frequency higher than the 200 kHz $1/f$ corner frequency of the laser intensity noise. If the microwave synthesizer is tuned to exactly the Nth harmonic of the laser pulse repetition frequency, the same point on the circuit waveform will be sampled every N cycles. The microwave frequency is then offset 10–100 Hz to map out the waveform at this rate. In this way, the sampler operates as a sampling oscilloscope. To use the sampler as a network analyzer, we remove the pulse modulation, offset the microwave frequency by 10 MHz, and replace the receiver with a narrow-band 10-MHz vector voltmeter. Using the sampler, we have investigated the causes of bandlimiting and gain compression in two microwave TWA's.

III. Amplifiers Tested

In a distributed amplifier, a series of small transistors are connected at regular spacings between two high-impedance transmission lines (Fig. 4). The high-impedance lines and the FET capacitances together form synthetic transmission lines, generally of 50-Ω characteristic impedance. Series stubs are used in the drain circuit, equalizing the phase velocities of the two lines and, at high frequencies, providing partial impedance matching of the drain output impedances and thus increasing the gain. By using small devices at small spacings, the cutoff frequencies due to the periodicities of the synthetic lines can be made larger than the bandwidth limitations associated with the line attenuations arising from FET gate and drain conductances; thus, gain–bandwidth products approaching f_{max} can be attained [6]. The amplifiers studied are a five-FET TWA for 2–18 GHz that uses microstrip transmission lines (Fig. 5) and a novel five-FET TWA for 2–20 GHz designed with coplanar waveguide transmission lines [7].

IV. Small-Signal Measurements

By driving the TWA input with a swept-frequency sinusoid of small amplitude and then positioning the laser probe near the FET gate and drain terminals, we measure the small-signal transfer function from the input to each of these nodes, showing relative drive levels at the FET gates and output levels at the FET drains.

Packaging problems were found in testing the coplanar TWA; the amplifier chip, which showed 5.5-dB gain to 19 GHz, gave 5-dB gain to only 8 GHz when bonded to microstrip transmission lines. The long ground current path between the chip and the microstrip ground planes

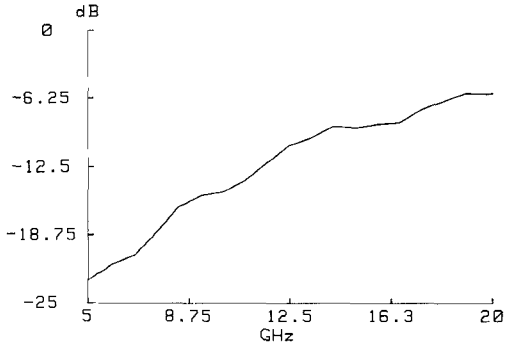

Fig. 6. Chip ground potential relative to carrier potential, as a fraction of input voltage on the coplanar TWA.

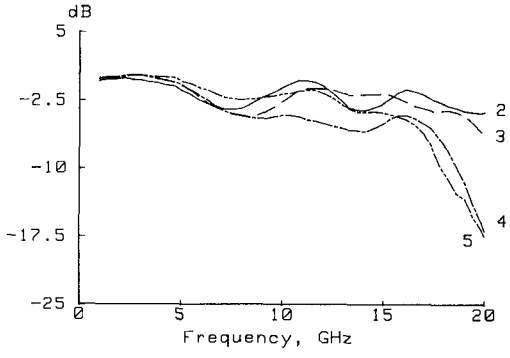

Fig. 7. Gate voltage versus frequency for the microstrip TWA, as a fraction of input voltage to amplifier; devices are numbered in order of propagation of forward wave. (Gate 1 omitted for clarity.)

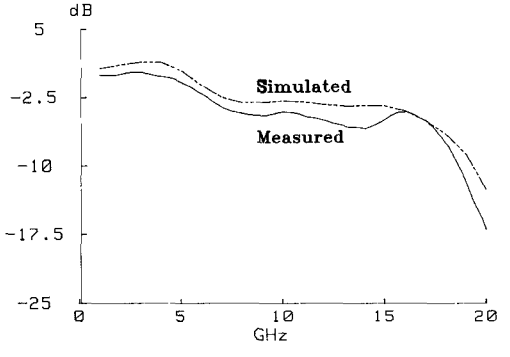

Fig. 8. Comparison between simulated and measured gate 4 voltage after adjustment of the model to obtain best fit to measurements.

was suspected; optically probing the potential between the chip and package ground planes showed that the chip ground potential is only 5 dB below the input signal at high frequencies (Fig. 6), indicating substantial package ground inductance. This inductance provides feedback and thus degrades gain. A package with coplanar waveguide transmission lines gave improved performance, but has not yet been optically probed.

The microstrip amplifier provides 6-dB gain to 18 GHz, while simulation predicts 7-dB gain to 20 GHz. The gate voltage curves for this amplifier (Fig. 7) show several features: the rolloff beyond 18 GHz is the cutoff of the synthetic gate line; the slow rolloff with frequency at gates 3, 4, and 5 is gate line attenuation; and the ripples are standing waves resulting from the gate line being mis-

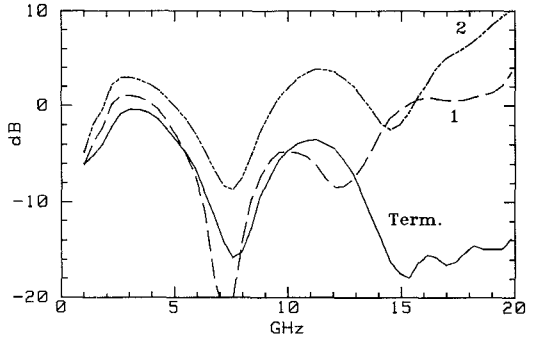

Fig. 9. Measured voltage at drain 2, drain 1, and drain reverse termination of microstrip TWA, as a fraction of input voltage.

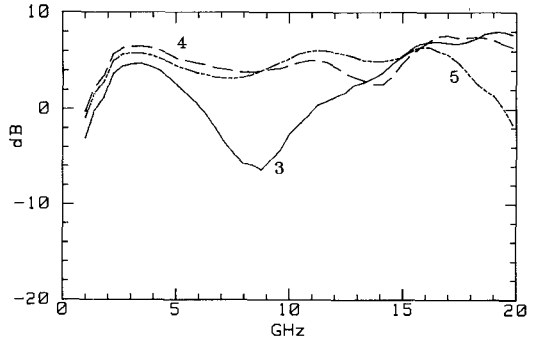

Fig. 10. Voltage versus frequency at drains 3, 4, and 5 of microstrip TWA

terminated. These data were compared to simulations using SuperCompact™; the simulator's optimizer was then used to adjust process-dependent circuit parameters to obtain the best fit to the measured data (Fig. 8). Model gate termination resistance increased to 80 Ω, C_{gs} increased from 1.0 to 1.14 pF/mm, C_{gd} increased from 0.03 to 0.06 pF/mm, source resistance r_s increased from 0.58 to 0.72 Ω, and source inductance decreased from 0.14 to 0.10 nH; these values fall within normal process variations. Interference between the forward and reverse waves on the drain line results in strong frequency dependence of the drain voltages (Figs. 9 and 10); this can be predicted by simple analysis.

V. Drain Voltage Distribution

After Ayasli [8], if the wavelength is much greater than the spacing between the FET's, the synthetic lines can be approximated as continuous structures coupled by a uniformly distributed transconductance. The lines then have characteristic impedances and phase velocities given by the sum of distributed and lumped capacitances and inductances per unit length [8]; the line impedances (Z_{0g}, Z_{0d}) and velocities (v_{pg}, v_{pd}) are generally made equal. The lines then have propagation constants given by

$$\gamma_g = \alpha_g + j\beta_g \simeq \frac{r_g \omega^2 C_{gs}^2 Z_{0g}}{2l} + j\omega/v_{pg} \tag{1}$$

$$\gamma_d = \alpha_d + j\beta_d \simeq \frac{Z_{0d} G_{ds}}{2l} + j\omega/v_{pd} \tag{2}$$

where l is the FET spacing, C_{gs} is the gate–source capaci-

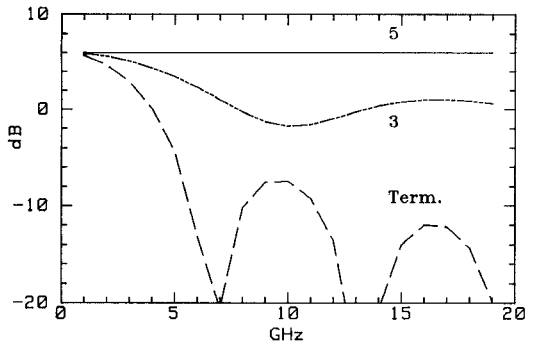

Fig. 11. Voltage versus frequency, referenced to input voltage, at drain 5, drain 3, and drain reverse termination as calculated by (4).

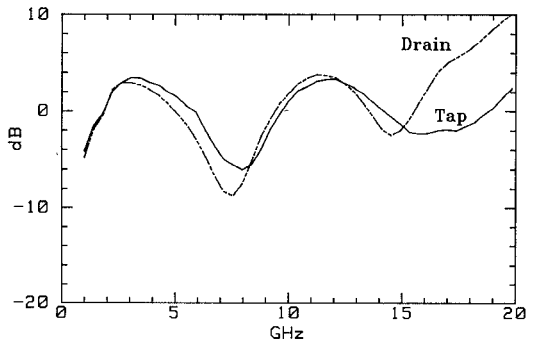

Fig. 12. Voltage versus frequency at drain 2 and at drain 2 tap point, microstrip amplifier.

tance, r_g is the gate resistance, G_{ds} is the drain–source conductance, and a forward propagating wave is of the form $e^{-\gamma z}$. The voltage along the drain line is

$$V_d(z) = \frac{-g_m Z_{0d} V_{\text{in}}}{2l} \cdot e^{-\gamma_g z}\left\{\frac{1-e^{(\gamma_g-\gamma_d)z}}{\gamma_d-\gamma_g} + \frac{1-e^{(\gamma_g+\gamma_d)(z-nl)}}{\gamma_d+\gamma_g}\right\} \quad (3)$$

where n is the number of FET's, g_m is the FET transconductance, V_{in} is the input voltage, and z is the distance along the drain line, with the origin located at the drain-line reverse termination. Ignoring line attenuation, and assuming equal gate and drain phase velocities, (3) becomes

$$\|V_d(z)\| = \frac{g_m Z_{0d} V_{\text{in}}}{2l} \cdot \sqrt{z^2 + z\frac{\sin(2\beta(nl-z))}{\beta} + \frac{\sin^2(\beta(nl-z))}{\beta^2}} \quad (4)$$

which is plotted in Fig. 11. The above analysis neglects the matching effect of the series drain stubs (Fig. 4). Because these series stubs provide partial high-frequency impedance matching between the FET's and the drain transmission line, at high frequencies the drain voltages are larger than the voltages at the tap points where the drain series stubs connect to the drain line (Fig. 12). Drain-line voltage variation also arises from reflections from the drain-line reverse termination, which, owing to process variations, was 80 Ω in the device tested. We see from Fig. 11 that at high frequencies the power absorbed by the drain-line reverse termination is about 20 dB below the amplifier output power. Furthermore, at high frequencies the input power is absorbed primarily in the FET input resistances and not in the gate-line termination. Thus, at high frequencies the TWA is a directional coupler with gain. The terminations reduce the low-frequency power gain but do not waste substantial available gain near the cutoff frequency. The predicted frequency-dependent drain voltage distributions also complicate the large-signal operation of the amplifier.

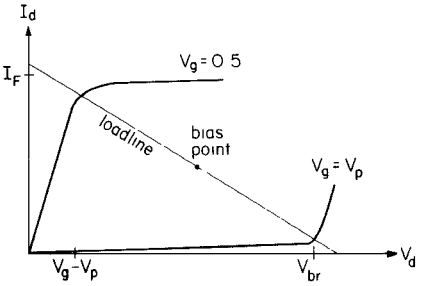

Fig. 13. FET load-line for maximum output power.

VI. Saturation Mechanisms

The nonlinearities and power limitations in FET amplifiers include gate forward conduction, pinchoff, drain saturation, and drain breakdown. Gate forward conduction, limiting the gate voltage for linear operation to a maximum of approximately +0.5 V, thus also limits the drain current to a maximum of I_F; the drain current at $V_{\text{gate}} = 0.5$ V. For linear operation, the gate voltage must also be more positive than the pinchoff voltage V_P and the drain voltage must be below the drain breakdown voltage V_{BR}. Finally, nonlinear operation results if the drain voltage is less than $(V_{\text{gate}} - V_P)$, the voltage necessary to pinch off the drain end of the FET channel; we refer to this as drain saturation.

In a single FET amplifier, the load-line can be chosen as in Fig. 13 so that all these limits are reached simultaneously, maximizing the output power before saturation. From this load-line, the gate and drain voltages must track in phase. Ayasli [9] and Ladbrooke [10] extend this result to traveling-wave amplifiers by assuming that under appropriate design conditions (tapered gate and drain lines) the gate voltages and drain voltages of all FET's can be made equal, thus causing all devices to saturate simultaneously. In the case where gate and drain losses can be neglected, we can show that if the drain and gate synthetic lines have characteristic impedances Z_{0d} and Z_{0g} and phase velocities v_{pd} and v_{pg} of the form

$$Z_{0d}(z) = K/z$$
$$Z_{0g}(z) = Z_0$$
$$v_{pd}(z) = v_{pg}(z) = v_p \quad (5)$$

and if the drain-line reverse termination is omitted and the output load resistance Z_{load} set at

$$Z_{\text{load}} = K/nl \quad (6)$$

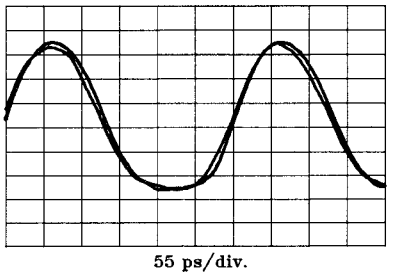

Fig. 14. Saturation at drains 4 and 5 of microstrip TWA; 3-GHz, 7-dBm input power.

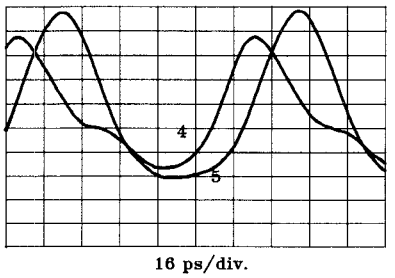

Fig. 15. Saturation at drains 4 and 5 of microstrip TWA; 10-GHz, 7-dBm input power

then the voltage along the drain line will be uniform as follows:

$$V_d(z) = -ng_m Z_{\text{load}} V_{\text{in}} e^{-j\omega z/v_p}. \tag{7}$$

The drain-line voltage is uniform and in phase with the gate-line voltage, allowing simultaneous saturation of all FET's and thus maximizing the output power at saturation.

In the uniform drain-line case, as is shown by (3) and by Figs. 9 and 10, the reverse wave on the drain line complicates the problem; the drain voltages are equal only at low frequencies, and, by (3), the reverse wave introduces a phase shift between the gate and drain voltages of each FET. Thus, in the uniform drain line case, neither the conditions for simultaneous saturation of all FET's nor the conditions for simultaneously reaching all saturation mechanisms in a given FET can be met.

The 2–18 GHz microstrip amplifier has 1-dB gain compression at 7-dBm input power, and is not optimized for maximum power output; the lines are not tapered in the form of (5) and the bias is not set for maximum uncompressed output power. Ignoring for a moment the frequency dependence and position dependence of the gate and drain voltages, we can estimate the gain compression point and identify the predominant saturation mechanism. With a gate bias voltage V_G of -0.3 V, a drain bias voltage V_D of 3.5 V, a pinchoff voltage of approximately -2 V, and an amplifier voltage gain of $A_V = -2$ (6 dB), the gate signal is $\delta V_{\text{gate}} = \delta V_{\text{drain}}/A_V$, and the maximum negative drain voltage excursion is limited by drain saturation to $\delta V_{\text{drain}} = -(V_D - V_G - |\delta V_{\text{gate}}| + V_P) = -1.2$ V corresponding to 11.5-dBm output power. With 6-dB amplifier gain, drain saturation will thus occur at input power levels of approximately 5.5 dBm, while the maximum input voltage before gate forward conduction occurs is $\delta V_{\text{gate}} = (0.5 - V_G) = 0.8$ V, corresponding to 8-dBm input power. As pinchoff and drain breakdown occur only at still higher input powers, the maximum power output of the amplifier is thus limited by drain saturation. Probing the drain and gate large-signal voltage waveforms with the amplifier driven at its 1-dB gain compression power, we observe no clipping of the gate voltage waveforms (which would arise from gate forward conduction), but observe clipping of the negative excursions of the drain voltage waveforms; the clipping resulting from drain saturation. Adjustment of the gate bias V_G to 0 V results in significant gate forward conduction at 7-dBm input power, and clipping of the positive excursions of the gate voltage waveforms was observed; subsequent tests were performed with the amplifier biased normally ($V_G = -0.3$ V), where gain compression is dominated by drain saturation.

At 3 GHz, the small-signal voltages at the drains of the last two devices are approximately equal, and are larger than the small-signal voltages at drains 1, 2, and 3 (see Figs. 9 and 10). Thus, clipping occurs simultaneously at drains 4 and 5 (Fig. 14). Because of the smaller voltage swings at drains 1, 2, and 3, these devices show strong drain saturation only at input power levels several decibels larger than the input power necessary to cause drain saturation in the fourth and fifth FET's.

At 10 GHz, the distortion at the 1-dB compression point is complicated by phase shifts between the 10-GHz fundamental and the 20-GHz generated harmonic currents (Fig. 15). The 10-GHz small-signal voltage at drain 5 is 1.5 dB larger than that at drain 4; thus, FET 5 saturates more strongly. As with the 3-GHz saturation characteristics, the 10-GHz small-signal voltages at drains 1, 2, and 3 are comparatively small, and thus the first three transistors do not show significant saturation at 1-dB gain compression. The 20-GHz harmonic current generated at FET 5 produces equal forward and reverse drain voltage waves at 20 GHz. With 10-ps line delay between drains 4 and 5, the 20-GHz reverse wave from FET 5 undergoes 20-ps relative phase delay (which is 72° of a 10-GHz cycle) before combining with the 10-GHz forward wave at drain 4. The resulting voltage waveform at drain 4 would then approximate a sawtooth function; drain saturation at FET 4 then clips the peak negative excursion. Depending upon the line delay between successive drains, the reverse-propagating harmonic currents can either increase or decrease the peak voltages at other drains, increasing or decreasing the saturation at prior devices.

At 18 GHz, the small-signal drain voltage at drain 4 is larger than that at drain 5. Thus, at the 1-dB gain compression point, FET 4 will saturate strongly while FET 5 will show only weak drain saturation. At this frequency, FET's 2 and 3 have small-signal drain voltages that are 0.5–1 dB smaller than at drain 4, and thus also show significant drain saturation. The 36-GHz harmonic currents generated at drain 4 are beyond the cutoff frequency of the synthetic drain line; the generated 36-GHz forward wave thus experiences significant dispersion and attenuation relative to

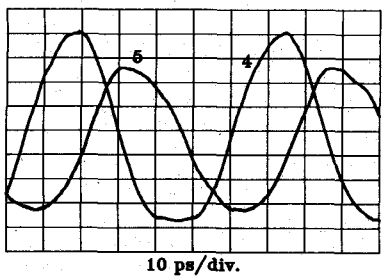

Fig. 16. Saturation at drains 4 and 5 of microstrip TWA; 18-GHz, 7-dBm input power.

the 18-GHz forward wave as the two waves propagate towards drain 5 and the output. The voltage waveform at drain 5 is thus visibly distorted, but the phase relationship between the fundamental and the distortion components has been shifted, and the waveform no longer clearly reflects the drain saturation waveform observed at drain 4 (Fig. 16).

VII. Conclusions

We have studied the propagation of signals internal to microwave distributed amplifiers with electrooptic sampling. Gate-line attenuation and cutoff is observed, as is interference of the forward and reverse wave on the drain lines, both as predicted by theory. Using a microwave simulation program, the circuit models can be adjusted to obtain a fit between simulated and measured internal node voltages, allowing detailed circuit diagnostics. Large-signal saturation characteristics of the amplifier are set by both the order of occurrence of each saturation mechanism in each FET, and by the propagation of the generated harmonic currents through the circuit.

Acknowledgment

The authors wish to thank G. Zdasiuk and C. Yuen of Varian Associates for their assistance. They also thank A. Macfarlane for typesetting the manuscript.

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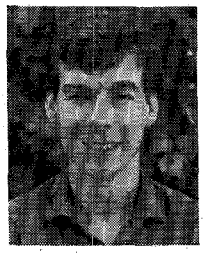

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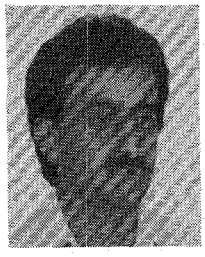
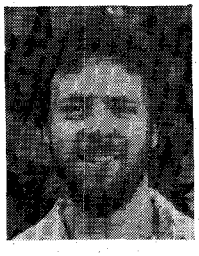
From 1982 through 1984, he worked at AT&T Bell Laboratories, designing fiber-optic digital transmission systems.



Majid Riaziat (M'84) received the B.S. degree in engineering physics from the University of Oklahoma, Norman, Oklahoma, in 1978 and the M.S. and the Ph.D. degrees in applied physics from Stanford University, Stanford, California, in 1980 and 1983, respectively.

In 1984, he joined Varian Research Center in Palo Alto, CA, where he is currently a Senior Engineer involved in MMIC design and microwave measurements research.



K. J. Weingarten (S'86) was born January 30, 1961 in St. Petersburg, FL. He received the B.S. degree in electrical engineering from the Georgia Institute of Technology, Atlanta, GA, in 1983 and the M.S. degree in electrical engineering from Stanford University, Stanford, CA, in 1985. He is currently a Ph.D. candidate in electrical engineering at Stanford.

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B. A. Auld (S'49–A'53–M'58–F'73) was born on November 4, 1922, in Wei-Hwei-Fu, China. He received the B.S. degree in electrical engineering from the University of British Columbia in 1946 and the Ph.D. degree in electrical engineering from Stanford University, Stanford, CA, in 1952.

In 1958, he joined the Edward L. Ginzton Laboratory, W. W. Hansen Laboratories of Physics, Stanford University, where he is currently a Professor of Applied Physics (research). His research activities have been concerned with electromagnetic and acoustic waves. Upon joining the staff at Edward L. Ginzton Laboratories, he worked on the application of nonlinear analysis to microwave ferrite problems, primarily with regard to parametric instabilities, harmonic generation, nonlinear resonance, and shock-wave propagation. In more recent years, he has been involved with microwave acoustics and acoustic imaging.

Dr. Auld was awarded the 1959 IRE Microwave Prize for a paper on symmetrical ferrite circulators. In 1983, he was awarded the IEEE Ultrasonic Achievement award for scientific excellence and distinction through contributions to ultrasonics.

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D. M. Bloom (S'68–M'76–M'80) was born on October 10, 1948, in Brooklyn, NY. He received the B.S. degree in electrical engineering from the University of California Santa Barbara in 1970 and the M.S. and the Ph.D. degrees in electrical engineering from Stanford University in 1972 and 1975, respectively.

From 1975 to 1977, he was employed by Stanford University as a Research Associate. During this period, he was awarded the IBM Postdoctoral Fellowship. From 1977 to 1979, he was employed by Bell Telephone Laboratories, Holmdel, NJ, where he conducted research on optical phase conjugation, ultrafast optical pulse propagation in fibers, and tunable color-center lasers. From 1979 to 1983, he served on the staff and later as a Project Manager at Hewlett Packard Laboratories, Palo Alto, CA. While at Hewlett Packard, he conducted and managed research on fiber-optical devices, high-speed photodetectors, and picosecond electronic measurement techniques. In late 1983, he joined the Edward L. Ginzton Laboratory, W. W. Hansen Laboratories of Physics, Stanford University, where he is currently an Associate Professor of Electrical Engineering. His current research interests are ultrafast optics and electronics.

He was awarded the 1980 Adolph Lomb Medal of the Optical Society of America for his pioneering work on the use of nonlinear optical processes to achieve real time conjugate wavefront generation. In 1981, he was elected a Fellow of the Optical Society of America in recognition of his distinguished service in the advancement of optics. He is the 1985 IEEE LEOS traveling lecturer.